GENERAL DESCRIPTION

The concept for the Texas Instruments Home Computer 99/4 or 99/4A I/O bus is to provide maximum flexibility and good performance with a constraint of low cost for both mainframe and computer system. This concept is achieved by providing both memory and CRU I/O buses to the 99/4 or 99/4A peripherals. This brief description will give key details of this interface. Detailed information regarding the 9900 CRU is assumed. A source for this information is the 9900 Family Systems Design and Data Book. This manual may be obtained from TI Semiconductor Distributors. The memory bus (with data bus converted to eight bits wide) is used for instruction fetch from ROM in external peripherals and for data transfer to/from memory mapped portions of these devices. The CRU bus is used for peripheral enable/disable and for device control and data transfer to/from CRU mapped peripherals.

A block diagram of the TI-99/4A electronics is shown in Figure A. The TMS 9900 microprocessor accesses each peripheral to obtain instructions from the device service routine (DSR) read only memory (ROM). Since each peripheral contains its own DSR, the 99/4A does not have to be designed to anticipate future peripheral requirements. The dual I/O bus capability, along with interrupt handling and external DSR's provide flexibility at low cost.

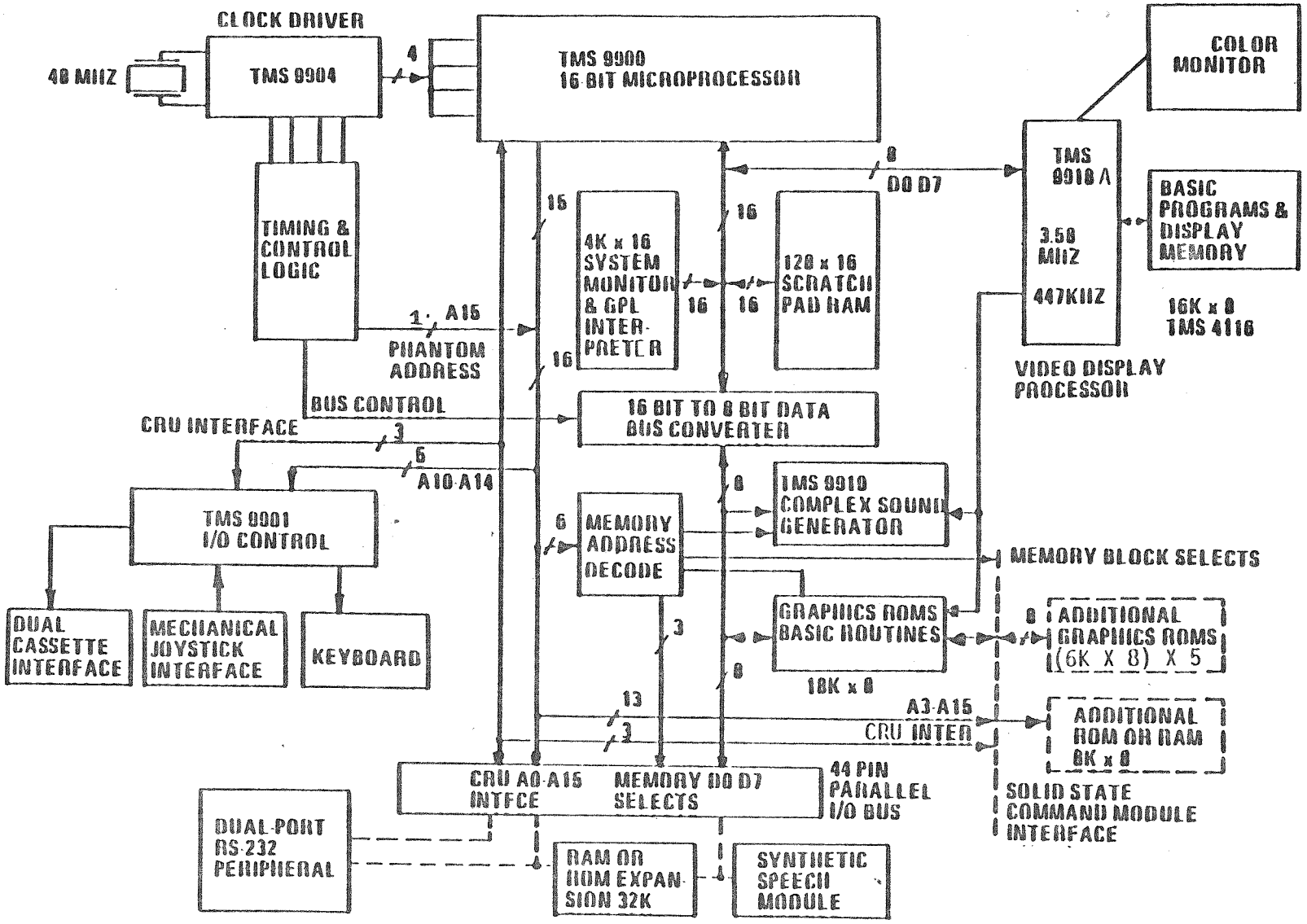
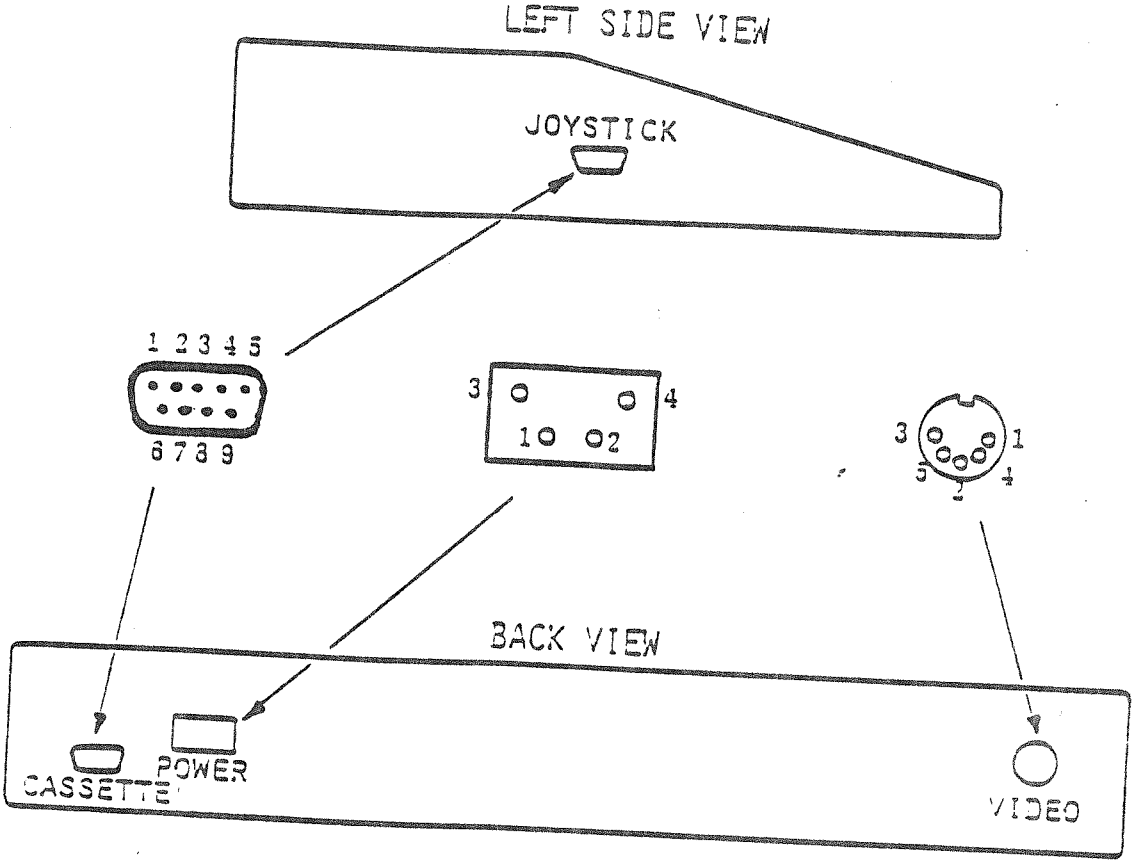


FIGURE A

SYSTEM BLOCK DIAGRAM



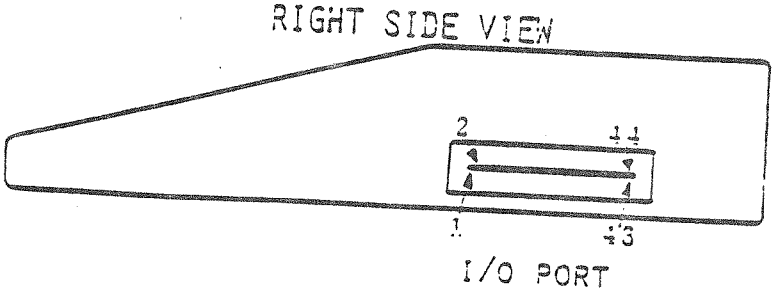


FIGURE E
CONNECTOR PIN IDENTIFICATION DIAGRAM

I1. MEMORY ALLOCATION

The memory address space is broken into 8 blocks of 8K bytes of memory. The third block (addresses 4000 - 5FFF) is predecoded and made available at the I/O port for the peripherals. The second, sixth, seventh, and eighth blocks (address 2000-3FFF and A000-FFFF) are in the memory expansion peripheral. For the speech module, (addresses 9000-97FF), a predecoded line is available at the I/O port.

SYSTEM MEMORY MAP

HEX ADDRESS

0 - 1FFF	Console ROM Space
2000 - 3FFF	Memory Expansion
4000 - 5FFF	Peripheral Expansion (predecoded to I/O Connector).
6000 - 7FFF	Command Module ROM/RAM (predecoded to GROM Connector.
8000 - 9FFF	Microprocessor RAM, VDP, GROM, SOUND and SPEECH select.
A000 - BFFF	Memory Expansion
C000 - DFFF	" "
E000 - FFFF	" "

MEMORY MAPPED DEVICES

ADDRESSES	A0	A1	A2	A3	A4	A5	A14	USE
8000	1	0	0	0	0	0	0	Internal RAM (8300-83FF)
8400	1	0	0	0	0	1	0	Sound
8800	1	0	0	0	1	0	0	VDP Read Data
8802	1	0	0	0	1	0	1	VDP Read Status
8C00	1	0	0	0	1	1	0	VDP Write Data
8C02	1	0	0	0	1	1	1	VDP Write ADDR.
9000	1	0	0	1	0	0	0	Speech Read
9400	1	0	0	1	0	1	0	Speech Write
9800	1	0	0	1	1	0	0	GROM Read Data
9802	1	0	0	1	1	0	1	GROM Read ADDR.
9C00	1	0	0	1	1	1	0	GROM Write Data
9C02	1	0	0	1	1	1	1	GROM Write ADDR.

Banks 1-7 available at other addresses, with external decode logic.

III. CRU ALLOCATION

Of the available 4K of CRU bits, the first 1K (addresses 0000-07FE) are used internally in the console. The second 1K (addresses 0800-0FFE) are reserved for future use. The last 1.9K (addresses 1000-1FFE) are reserved for the peripherals to be plugged in the I/O port. A block of 128 CRU bits is assigned to each peripheral as listed below.

CRU ASSIGNMENTS

CRU ADDRESS	A3	A4	A5	A6	A7	USE
0000-0FFE	0	X	X	X	X	Internal Use
1000-10FE	1	0	0	0	0	Hard Disk Controller
1100-11FE	1	0	0	0	1	Disk Controller
1200-12FE	1	0	0	1	0	Modems
1300-13FE	1	0	0	1	1	RS232 (I)
1400-14FE	1	0	1	0	0	Reserved
1500-15FE	1	0	1	0	1	RS232 (II)
1600-16FE	1	0	1	1	0	Reserved
1700-17FE	1	0	1	1	1	Reserved
1800-18FE	1	1	0	0	0	Thermal Printer
1900-19FE	1	1	0	0	1	Unassigned
1A00-1AFE	1	1	0	1	0	Reserved
1B00-1BFE	1	1	0	1	1	Debugger
1C00-1CFE	1	1	1	0	0	VCR Controller
1D00-1DFE	1	1	1	0	1	IEEE 488 Bus Controller
1E00-1EFE	1	1	1	1	0	Reserved
1F00-1FFE	1	1	1	1	1	P-Code

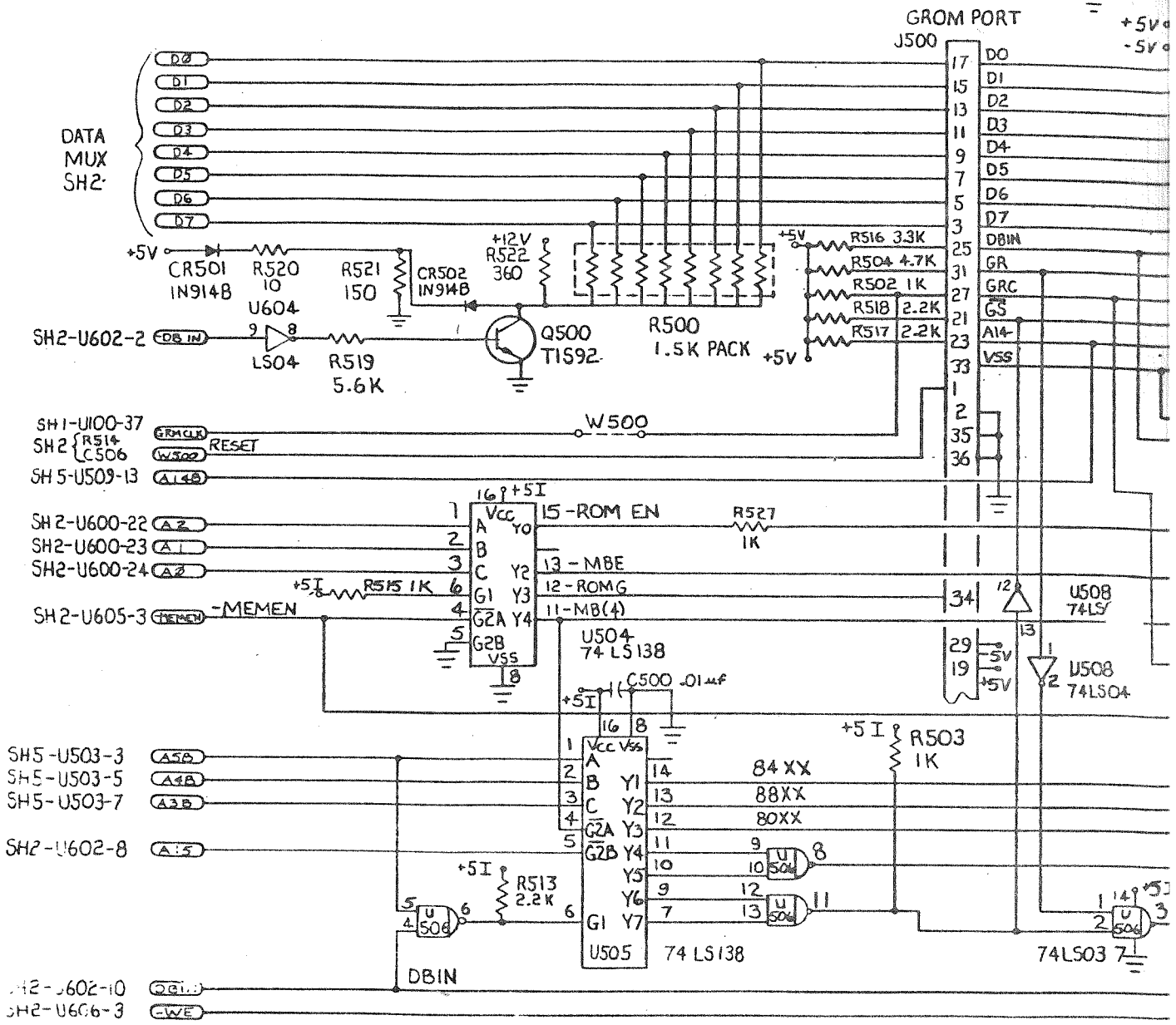
IV. INTERRUPT HANDLING

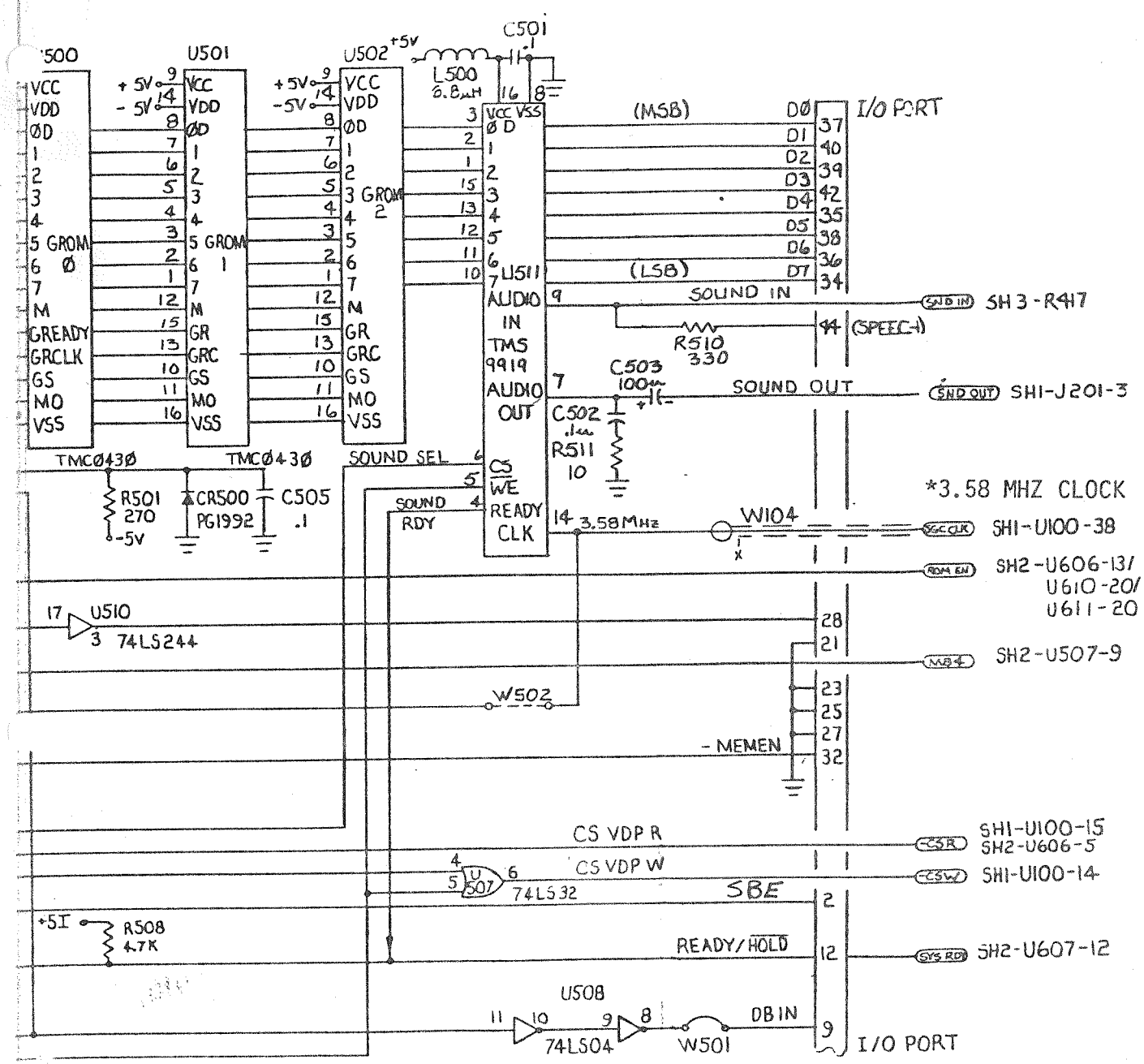
The interrupt available on the I/O port is one of the maskable interrupts of the TMS 9901 Programmable System Interface.

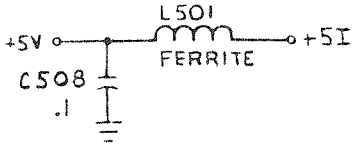
9900 INTERRUPTS

INTERRUPT LEVEL	VECTOR LOC. (MEMORY ADDR. IN HEX)	CPU PIN	DEVICE ASSIGNMENT
(Highest Priority)	0000-WSP 0002-PC	RESET	RESET
0	FFFC-WSP FFFE-PC	LOAD	LOAD
1	0004-WSP 0006-PC	--	EX DEV (9901)

Lower priority CPU interrupts are not used. The additional interrupts are implemented on the 9901. Interrupt Level 1 is decoded by software to be either (1) VDP vertical sync. (2) 9901 internal timer or (3) I/O bus-generated.

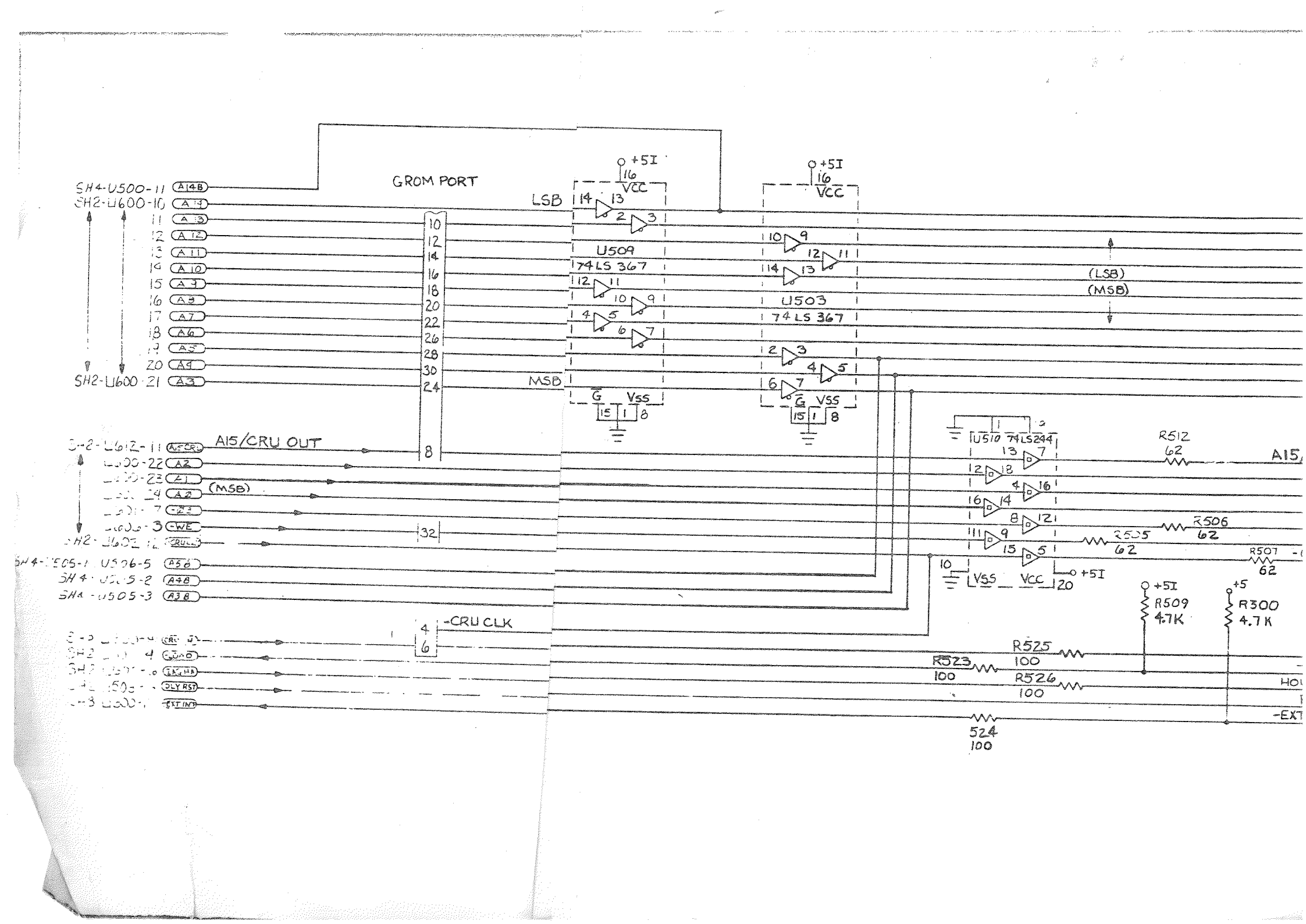

GROM PORT
J500
DATA MUX SH2-
D0
D1
D2
D3
D4
D5
D6
D7
+5V
CR501 IN914B
R520 10
U604
R521 150
CR502 IN914B
+12V
R522 360
R500 1.5K PACK
Q500 T1592
SH2-U602-2
-DB IN
LS04
R519 5.6K
R516 3.3K
R504 4.7K
R502 1K
R518 2.2K
R517 2.2K
DBIN
GR
GRC
GS
A14-
VSS
SH1-U100-37
GRMCLK
SH2 R514 C506
RESET
W500
SH5-U509-13
A14B
SH2-U600-22
SH2-U600-23
SH2-U600-24
A2
A1
A0
R515 1K
SH2-U605-3
MEMEN
-MEMEN
U504
74 LS138
15 -ROM EN
R527 1K
13 - MBE
12 - ROMG
11 - MB(4)
C500 .01 uf
U508
74LS
74LS04
SH5-U503-3
SH5-U503-5
SH5-U503-7
A5B
A4B
A3B
SH2-U602-8
A15
R503 1K
84XX
88XX
80XX
R513 2.2K
U506
U505
74 LS138
74LS03
DBIN
SH2-U602-10
SH2-U606-3
CWE





*SN76489 USES 3.58 MHZ CLOCK
SUPPLIED THRU W104 COAX
SN94624 USES 447 KHZ
SUPPLIED THRU W502

TEXAS INSTRUMENTS | DWN | DATE 12/1/79 | ISSUE DATE | SIZE D | FSCM NO 96214 | DWG NO 1039025


GROM PORT
LSB
MSB
U509
74LS 367
U503
74LS 367
+5I
VCC
VSS
(LSB)
(MSB)
A15/CRU OUT
-CRU CLK
U510 74LS244
R512
62
R506
62
R505
62
R507
62
R509
4.7K
R300
4.7 K
R525
100
R523
100
R526
100
524
100
SH4-U500-11
SH2-U600-10
SH2-U600-21
SH2-U612-11
SH4-U505-1
SH4-U505-2
SH4-U505-3
-EXT